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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,969	09/22/2003	Katsumi Abe	Q75817	4962
23373 7590 02/02/2007 SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER PHAM, TAMMY T	
			ART UNIT 2629	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE 3 MONTHS			MAIL DATE 02/02/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/664,969

Applicant(s)

ABE, KATSUMI

Examiner

Tammy Pham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7, 16-21, 27 and 28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 16-21, 27 and 28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

Claims 8-15, 22-26 have been withdrawn. Claims 1 and 16 have been amended. Claims 27-28 have been added. Claims 1-7, 16-21, 27-28 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 27 are rejected under 35 U.S.C. 102(b) as being anticipated by KUMADA et al. (US Application No: 2002/0008686 A1).

As for independent claims 1, KUMADA teaches of a common drive circuit (*Fig. 2, item 10 and Fig. 3*) for a display (*Fig. 2*), the common drive circuit (*Fig. 2, item 10 and Fig. 3*): comprising: a first voltage supply (*Fig. 3, item "positive power source"*) and a second voltage supply (*Fig. 3, item GND*) which respectively supply a high level voltage signal (*Fig. 3, item Vdd*) and a low level voltage signal (*Fig. 3, item GND*) to a common electrode (*Fig. 3, item "common electrode," section [0051]*); at least one first transistor (*Fig. 3, un-numbered item consisting of top transistor*) including either a drain or a source terminal connected to the first

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voltage supply (Fig. 3, item "positive power source"); at least one second transistor (Fig. 3, un-numbered item consisting of bottom transistor) including either a drain or source terminal connected to the second voltage supply (Fig. 3, item GND); at least one signal line (Fig. 3, un-numbered item where *V_{in}* enters) connected to each gate terminal of the first and second transistor (Fig. 3, un-numbered item consisting of transistors, section [0050]); and at least one capacitance load (Fig. 3, item "to liquid crystal panel," and in Fig. 2, item 1) connected to respective terminals of the first and the second transistors (Fig. 3, un-numbered item consisting of transistors) not connected to the first and second voltage supplies (Fig. 3, items *V_{dd}* and *GND*, respectively, section [0043]), wherein a high level of a signal (Fig. 3, item *V_{dd}*) passing through the at least one signal line (Fig. 3, item *V_{in}*) is the same or higher than the high level voltage signal (Fig. 3, item *V_{dd}*) supplied by the first voltage supply (Fig. 3, item "positive power source") and a low level (Fig. 3, item *GND*) of the signal passing through the signal line (Fig. 3, un-numbered item where *V_{in}* enters) is the same or lower than the low level voltage signal (Fig. 3, item *GND*) supplied by the second voltage supply (Fig. 3, item *GND*) in section [0050].

As for claim 3, KUMADA teaches that the at least one first transistor (Fig. 3, un-numbered item consisting of top transistor) comprises P-type transistor and the at least one second transistors (Fig. 3, un-numbered item consisting of bottom transistor) comprises N-type transistor, and wherein the gate terminals of the first and second transistors (Fig. 3, un-numbered item consisting of transistors) are connected to common signal lines (Fig. 3, item "common electrode signal") in section [0049]. (NOTE: That KUMADA points that the Fig. 3 consists of

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C-MOS switches. However, C-MOS switches uses complementary and symmetrical pairs of p-type and n-type MOSFETS for logic functions, aka the MOSFETS are connected in parallel).

As for claim 27, KUMADA teaches that the high level voltage signal (Fig. 3, item Vdd) supplied by the first voltage supply (Fig. 3, item "positive power source") is a high level common voltage (VCOMH) (Fig. 3, item Vdd) and the low level voltage signal (Fig. 3, item GND) supplied by the second voltage supply (Fig. 3, item GND) is a low level common voltage (VCOML) (Fig. 3, item GND), which are respectively supplied to the common electrode (VCOM) in Fig. 3 and in section [0050].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 4-7, 16-21, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over

KUMADA et al. (US Application No: 2002/0008686 A1).

As for independent claims 2, 16, KUMADA teaches of a display (Fig. 2) comprising: a substrate; a display portion (Fig. 2, item 1) integrated on the substrate (Fig. 2); and a gate driver circuit (Fig. 2, item 2), which controls switching of pixels (Fig. 2, item 7) of each line (Fig. 2,

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item G(1-M)) in a display portion (Fig. 2, item 1); a common drive circuit (Fig. 2, item 10) for the display portion (Fig. 2, item 1) for-which simultaneously driving capacitance loads (Fig. 2, item 1) in Fig. 2.

KUMADA fails to teach that the display portion (Fig. 2, item 1), wherein the common drive circuit (Fig. 2, item 10) is disposed on a position opposite to the gate driver circuit (Fig. 2, item 2) and the display portion (Fig. 2, item 1) therebetween.

Applicant has not disclosed any specific advantage or criticality to having the common drive circuit position opposite to the gate driver circuit and placing the display portion in between. As such, having the common drive circuit position opposite to the gate driver circuit and placing the display portion in between is an obvious matter of design choice.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to position the common drive circuit opposite to the gate driver circuit and placing the display portion in between because moving the common driver so it is at the opposite end from the gate driver (for example, right side of the display (1) of Fig. 2) would still allow the display to function as specified. "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).

As for claim 17, KUMADA teaches of a common drive circuit (Fig. 2, item 10 and Fig. 3) for a display (Fig. 2), the common drive circuit (Fig. 2, item 10 and Fig. 3): comprising: a first voltage supply (Fig. 3, item "positive power source") and a second voltage supply (Fig. 3, item GND) which respectively supply a high level voltage signal (Fig. 3, item Vdd) and a low level voltage signal (Fig. 3, item GND) to a common electrode (Fig. 3, item "common electrode," section [0051]); at least one first transistor (Fig. 3, un-numbered item consisting of top transistor) including either a drain or a source terminal connected to the first voltage supply (Fig. 3, item "positive power source"); at least one second transistor (Fig. 3, un-numbered item consisting of bottom transistor) including either a drain or source terminal connected to the second voltage supply (Fig. 3, item GND); at least one signal line (Fig. 3, un-numbered item where Vin enters) connected to each gate terminal of the first and second transistor (Fig. 3, un-numbered item consisting of transistors, section [0050]); and at least one capacitance load (Fig. 3, item "to liquid crystal panel," and in Fig. 2, item 1) connected to respective terminals of the first and the second transistors (Fig. 3, un-numbered item consisting of transistors) not connected to the first and second voltage supplies (Fig. 3, items Vdd and GND, respectively, section [0043]), wherein a high level of a signal (Fig. 3, item Vdd) passing through the at least one signal line (Fig. 3, item Vin) is the same or higher than the high level voltage signal (Fig. 3, item Vdd) supplied by the first voltage supply (Fig. 3, item "positive power source") and a low level (Fig. 3, item GND) of the signal passing through the signal line (Fig. 3, un-numbered item where Vin enters) is the same or lower than the low level voltage signal (Fig. 3, item GND) supplied by the second voltage supply (Fig. 3, item GND) in section [0050].

As for claims 4, 19, KUMADA teaches that P-type transistors and N-type transistors are connected in parallel to be the first transistor (Fig. 3, un-numbered item consisting of the top transistor), and N-type transistors and P-type transistors are connected in parallel to be the second transistor (Fig. 3, un-numbered item consisting of the bottom transistor), wherein respective gates of the P-type transistors of the first transistor (Fig. 3, un-numbered item consisting of the top transistor) and the N-type transistor of the second transistors (Fig. 3, un-numbered item consisting of the bottom transistor) are connected to one the signal line (Fig. 3, un-numbered item in which V_{in} is coming in from), and respective gates of the N-type transistors of the first transistor (Fig. 3, un-numbered item consisting of the top transistor) and the P-type transistors of the second transistor (Fig. 3, un-numbered item consisting of the bottom transistor) are connected to an inversion signal line (*NOTE: That since a C-MOS consist of a pair of p-type and n-type connected in parallel; the p-type is typically is active when the current is in an unconventional mode, in other words, can the p-type can be seen as connected to an inverted signal*) of one the signal line (Fig. 3, un-numbered item in which V_{in} is coming in from) in Fig. 3 and in section [0049]. (*NOTE: That KUMADA points that the Fig. 3 consists of C-MOS switches. However, C-MOS switches uses complementary and symmetrical pairs of p-type and n-type MOSFETS for logic functions, aka the MOSFETS rae connected in parallel*).

As for claims 5, 20, KUMADA teaches that a high-level voltage (not shown) of each signal of the signal line (Fig. 2, items G(1-M)) and the inversion signal line (Fig. 6, item coming from 81) is a high-level line voltage (not shown) of the gate driver (Fig. 2, item 2) and wherein a low-level voltage (Fig. 3, item GND) of each signal of the signal line (Fig. 2, items

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G(I-M)) and the inversion signal line (Fig. 6, item coming from 81) is a low-level line voltage (not shown) of the gate driver (Fig. 2, item 2) in sections [0143, 0148]. *(NOTE: That section [0143] teaches that scan signals from the gate driver are used to adjust the voltage levels of all of the source signals supplied by the source driver for all pixels electrodes. All of the source signals includes signals such as Vdd from the positive power source in Fig. 3 that is considered to be the high-level voltage in the common driver of Fig. 3).*

As for claims 6, 21, KUMADA teaches that the first (Fig. 3, un-numbered item consisting of the top transistor) and second transistors (Fig. 3, un-numbered item consisting of the bottom transistor) are comprised of thin-film transistors in sections [0004-5].

As for claim 7, KUMADA teaches that the display portion comprises a liquid crystal display (Fig. 2) in section [0002].

As for claim 18, KUMADA teaches that the at least one first transistor (Fig. 3, un-numbered item consisting of top transistor) comprises P-type transistor and the at least one second transistors (Fig. 3, un-numbered item consisting of bottom transistor) comprises N-type transistor, and wherein the gate terminals of the first and second transistors (Fig. 3, un-numbered item consisting of transistors) are connected to common signal lines (Fig. 3, item "common electrode signal") in section [0049]. *(NOTE: That KUMADA points that the Fig. 3 consists of C-MOS switches. However, C-MOS switches uses complementary and symmetrical pairs of p-type and n-type MOSFETS for logic functions, aka the MOSFETS rae connected in parallel).*

As for claim 28, KUMADA teaches that the high level voltage signal (Fig. 3, item Vdd) supplied by the first voltage supply (Fig. 3, item "positive power source") is a high level common voltage (VCOMH) (Fig. 3, item Vdd) and the low level voltage signal (Fig. 3, item GND) supplied by the second voltage supply (Fig. 3, item GND) is a low level common voltage (VCOML) (Fig. 3, item GND), which are respectively supplied to the common electrode (VCOM) in Fig. 3 and in section [0050].

Response to Arguments

Applicant's arguments with respect to claims 1-7, 16-21, 27-28 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
January 30, 2007


JEREMY NGUYEN
PRIMARY EXAMINER


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